Name of Teaching Staff	:	Prof.(Mrs.) Poonam Kadam
Designation	:	Assistant Professor
Department	:	Electronics & Telecommunication Engineering
Date of Joining the Institution	:	2.2.2006
Qualifications with Class / Grade	:	1. M.Tech (Microelectronics) from Banaras Hindu University with 1st Class Distinction in June 2003 CGPA 9.13. 2. B.E. (Electronics Engineering) in May/June 2001 from Swami Ramanand Tirth Marathwada University with 76.30%, 1st Class Distinction.
Total Experience in Years	:	Teaching: 12 years

1. Assistant Professor in EXTC Dept at D. J. Sanghvi College of Engineering from 2.7.2007 till date.
2. Adhoc faculty in IT Dept at D. J. Sanghvi College of Engineering from 2.2.2006 -2.7.2007.
3. Lecturer in I.T., D. J. Sanghvi College of Engineering from 3.2.2006 to 30.06.2006 and from 11.7.2006 to 01.7.2007.
4. Lecturer at S.G.G.S Institute of Technology from 3.2.2003 to Jan 2006.

Industry: --

Research: --

Papers Published : National: 5

International: 3

Published a paper titled “Efficient data path designing using Conservative logic” in world scientific & Engineering Academy and society Journal (International Journal).

Published a paper titled “Efficient data path designing using Conservative logic” in world scientific & Engineering Academy and society Conference Proceeding.

Poonam Kadam, Amrita Oza,”Techniques for Sub-threshold Leakage Reduction in Low Power CMOS Circuit Designs , **IJCA July 2014 Edition** with effect from **July 18, 2014**.

Papers Presented in Conferences	:	National: 5

1. Poonam Varma, V. Shahane, "Efficient VLSI computing paradigm using a Novel 5*5 Universal Reversible gate", DJSCOE & NMIMS – National conference on information and communication Technology New Horizon in Technology and Applications, PP.4, March 01-03, 2007.
2. Poonam Kadam, Aksheit J, Bhavin M, Ronak H, "Multiplier design using SCRL technique" – NCCT 2011.
3. FPGA implementation of AES algorithm using VHDL, Technofocus.
4. Aruna Rani and Poonam Kadam , "Adiabatic Split Level Charge Recovery Logic Circuit", International Journal of Computer Applications(IJCA) 65(25)18-22 March 2013.
5. Aruna Rani and Poonam Kadam,"Split level charge recovery logic"Proceedings of national Conference on VLSI & Image Processing ,NCVLSI'13, March 2013.

International: 1

Poonam Varma, V. Mohan, A. Joge, "Efficient data path designing using Reversible Conservative logic", 8th WSEAS International conference on circuits and system, 2004, Published in WSEAS Proceedings, issue 5, valance 3, PP. 1161-66, July 04.

PhD Guide ? Give field & University	:	Field:	--
		University:	--
PhDs / Projects Guided	:	PhDs :	--

Projects at Masters level:

Projects Guided : 1 completed

3 pursuing

Books Published / IPRs / Patents	:	1. VLSI Design (MU) Techmax 2. Advanced VLSI Design (MU) Techmax Publication. 3. VLSI Design and Technology (GTU) Techmax Publication. 4. VLSI Design and Technology, Pune University, Techmax Publication.
Professional Memberships	:	ISTE lifetime Membership
Consultancy Activities	:	--
Awards	:	--
Grants fetched	:	--
Interaction with Professional Institutions	:	--